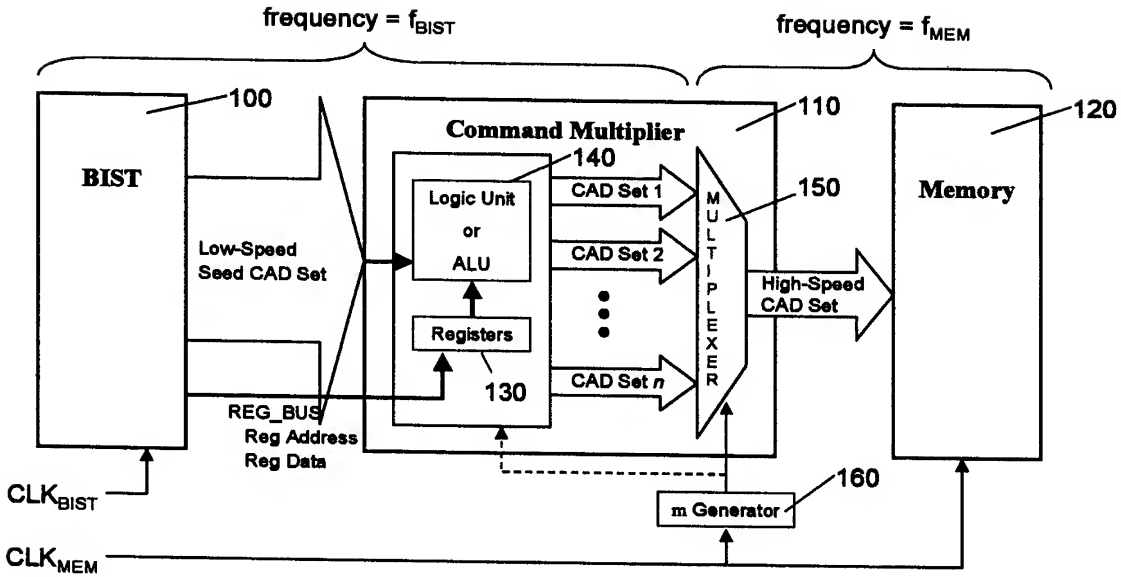

Figure 1

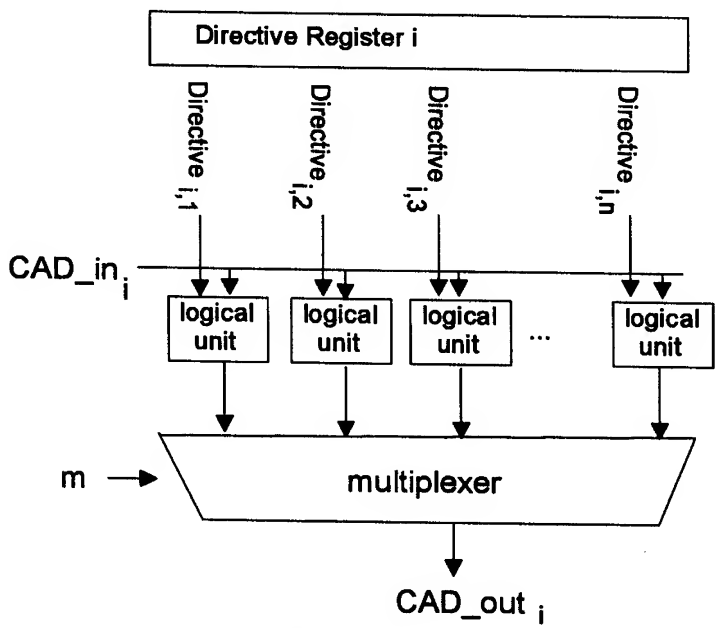

Figure 2

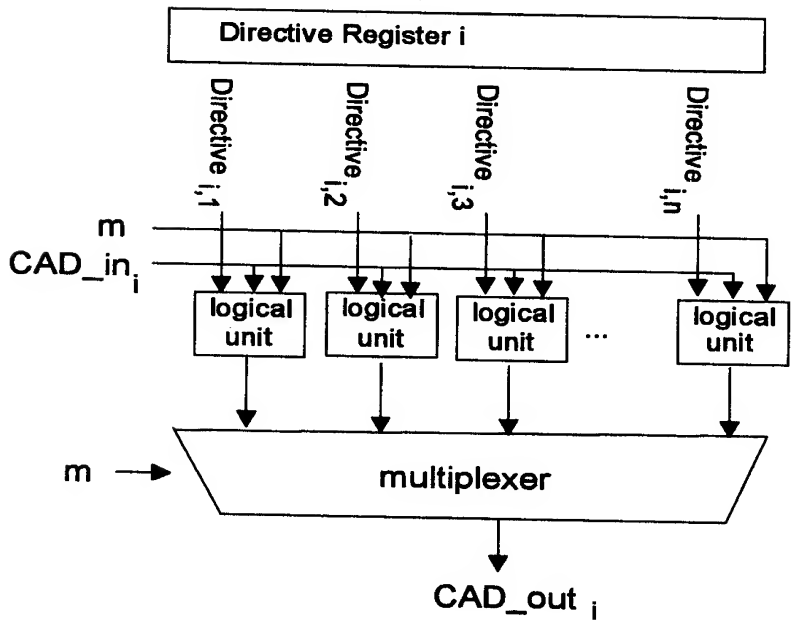

Figure 3

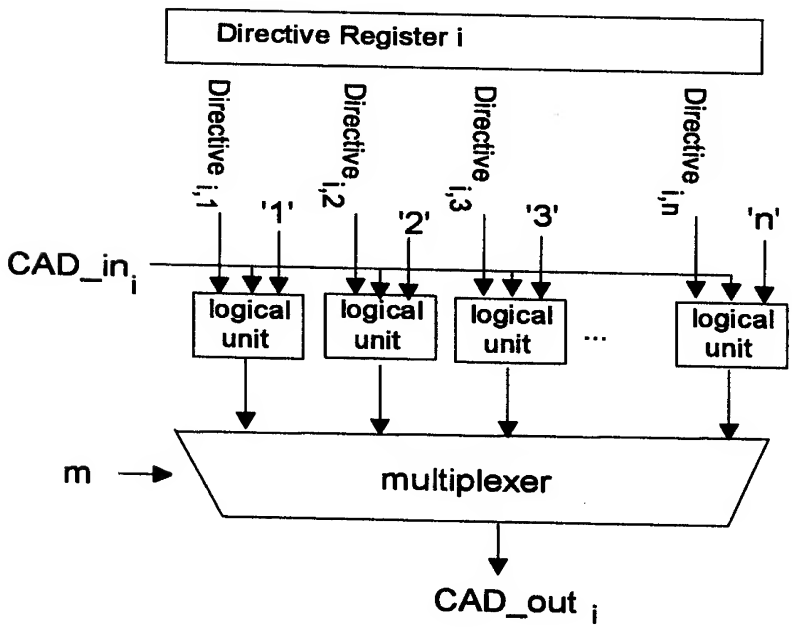

Figure 4

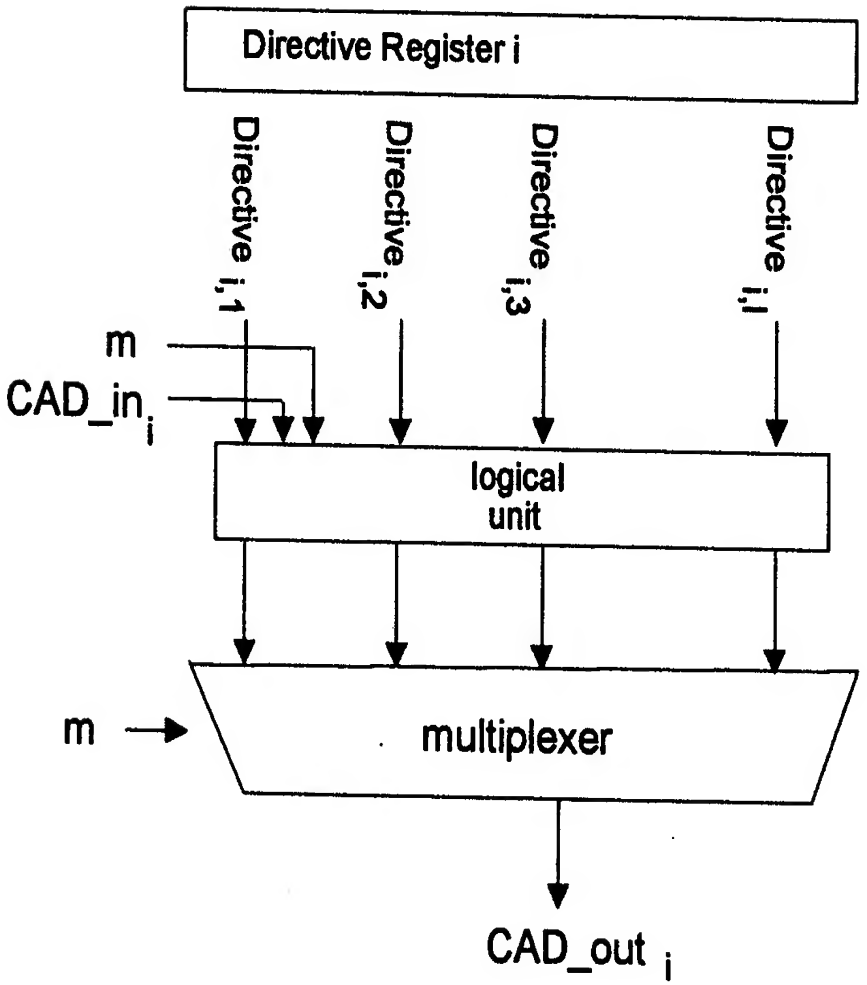
Directive Register i
Directive i,1
Directive i,2
Directive i,3
Directive i,l
m
CAD_in i
logical unit
m
multiplexer
CAD_out i

Figure 5

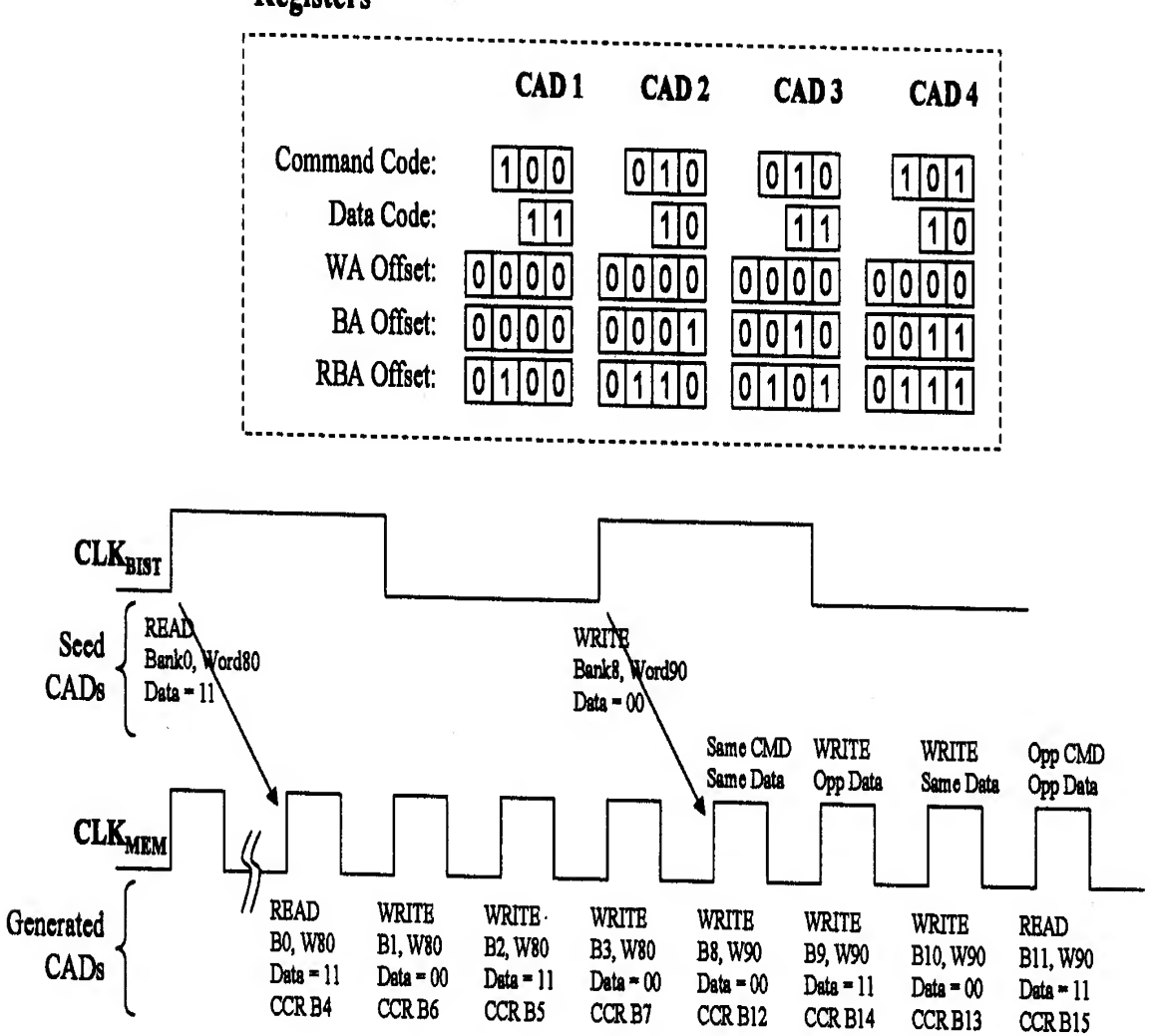
Registers
CAD 1
CAD 2
CAD 3
CAD 4
Command Code:
Data Code:
WA Offset:
BA Offset:
RBA Offset:
1 0 0
1 1
0 0 0 0
0 1 0 0
0 1 0
1 0
0 0 0 0
0 1 1 0
0 1 0
1 1
0 0 0 0
0 1 0 1
1 0 1
1 0
0 0 0 0
0 1 1 1
CLK BIST
Seed CADs
READ Bank0, Word80 Data = 11
WRITE Bank8, Word90 Data = 00
Same CMD Same Data
WRITE Opp Data
WRITE Same Data
Opp CMD Opp Data
CLK MEM
Generated CADs
READ B0, W80 Data = 11 CCR B4
WRITE B1, W80 Data = 00 CCR B6
WRITE B2, W80 Data = 11 CCR B5
WRITE B3, W80 Data = 00 CCR B7
WRITE B8, W90 Data = 00 CCR B12
WRITE B9, W90 Data = 11 CCR B14
WRITE B10, W90 Data = 00 CCR B13
READ B11, W90 Data = 11 CCR B15

Figure 6

Sample CMX Command Op Codes

Op Code	Operation
000	NOP (seed independent)
001	READ (seed independent)
010	WRITE (seed independent)
011	*Unused*
100	Same Command as Seed
101	Opposite Command to Seed
110	*Unused*
111	*Unused*

Sample CMX Data Op Codes

Op Code	Operation
00	00 (independent of seed)
01	11 (independent of seed)
10	Opposite Data from Seed
11	Same Data as Seed

Figure 7